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Low Power Multi-Bit Flip-Flops Design for VLSI Applications

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Abstract-
The utilization of power has turned into a smoldering issue in current VLSI design. Power consumption can be lessened by substituting some flip-flops with less multi-bit flip-flops. Multi-bit flip-flops are one of the strategies for reducing the clock power consumption. This project concentrates on diminishment of clock force utilizing multi-bit flip-flops by clock synchronization. Diminishment of the clock power consumption with two single bit flip-flops are synchronized with single clock pulse. Uniting single bit flip-flops into one multi-bit flip-flop evades duplicate inverters, brings down the aggregate clock power utilization which lessens the total area. A mixture table is fabricated to acquire a multi-bit flip-flop which can store the flip-flops that can be consolidated. This task concentrates on D flip-flop which builds the loading of the clock signal. QCL adder is utilized as an application for multi-bit flip-flop. Highest '1' bit finding algorithm is utilized to discover the highest 1 bit from the yield of QCL adder. This calculation checks the yield of QCL adder in each one cycle.
Keywords: QCL, SOC, Mbffs, merging, power reduction, clock buffer.

I.INTRODUCTION

Because of the prominence of compact electronic items, low power framework has pulled in more consideration lately. As technology advances, a system-on-a-chip (SOC) configuration can contain more parts that prompt a higher power density. This makes power dissipation achieve the cutoff points of what packaging, cooling or other framework can help. Decreasing the power consumption can upgrade battery life as well as can evade the overheating issue, which would build the level of trouble of packaging or cooling consequently, the thought of power consumption in complex SOCs has turned into a huge test to designers. In addition, in advanced VLSI plans, power consumed by clocking has taken a significant piece of the entire plan particularly for those designs using deeply scaled CMOS technologies. In this way, a few strategies have been proposed to decrease the power consumption of clocking.

For a given plan that the areas of the cells have been firm, the power consumed by clocking can be decreased further by substituting a few flip-flops with multi-bit flip-flops. At clock tree synthesis, less number of flip-flops implies reduced number of clock sinks. Therefore, the resulting clock system uses reduced power consumption and utilizes less routing resource.

Furthermore, smaller flip-flops are substituted by bigger multi-bit flip-flops; gadget varieties in the relating circuit can be orderly reduced. As the CMOS technology progresses, the driving capacity of an inverter-based clock buffer increments fundamentally. The ability to drive a clock buffer can be assessed by the quantity of least measured inverters that it can drive on a given rising or falling time. Due to this sensation, a few flip-flops can impart a common clock buffer to evade unnecessary waste of power.

Fig. 1 shows the block diagrams of 1- and 2-bit flip-flops. If we replace the two 1-bit flip-flops as shown in Fig. 1(a) by the 2-bit flip-flop as shown in Fig. 1(b), the total power consumption can be reduced because the two 1-bit flip-flops can share the same clock buffer.

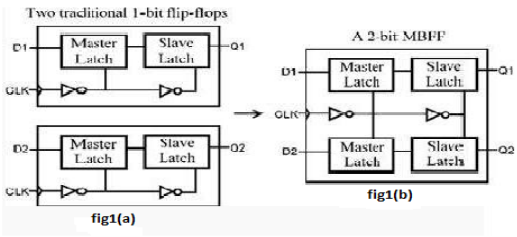

Fig.1: Example of merging two 1-bit flip-flops into one 2-bit flip-flop.(a) Two 1-bit flip-flops (before merging). (b) 2-bit flip-flop (after merging)

In any case, the areas of some flip-flops would be changed after this substitution, and subsequently

the wire lengths of nets connecting pins to a flip-flop are additionally changed. To abstain from damaging the timing imperatives, we confine that the wire lengths of nets uniting pins to a flip-flop can't be longer than detailed values after this procedure. On the other hand, to ensure that another flip-flop can be put inside the desired region, we likewise need to consider the area capacity of the region.

The power plays a significant part in any design one may need to focus on power reduction strategies. To diminish the power consumption, a lot of low-power plan procedures have been presented, for example, clock gating, power gating making multi-supply-voltage plans, dynamic voltage per frequency scaling, and minimizing clock system. Among these procedures, minimizing and fusing the clock system is essential in reducing power consumption of a Soc (System on Chip). By diminishing the power in circuit design it naturally reduces the many-sided quality and wire length. In this manner, distinctive systems have been proposed [2], [3] to design a reduced power consumption design.

The power had been expanded for diverse stages are static and dynamic power. In dynamic power, change in input signal at distinctive rationale level will result in exchanging and short out force in the configuration. In static force, it doesn't have any impact of level change in information and yield. The Multi-bit Flip-flop (MBFF) is a successful power reduction procedure. It is utilized to decrease the quantity of Flip Flop away stage. Sending numerous bits of information with single FF utilizing single clock pulse is called MBFF. The idea of MBFF is presented in adder application which is utilized to diminish the quantity of FFs which are not empowered in the circuit outline. Mbffs have advantage over SBFF as more modest outline zone, controllable clock, less delay on clock system and effective use of routing resources.

The working of multi-bit flip flop is same as single-bit flip-flop, at whatever point the clock gets dynamic state flip flop latches all data to yield. For idle state the flip flop holds the information. The fundamental structure of multi-bit flip failure is given in Fig. 1, it demonstrates that as opposed to utilizing single bit FF we can supplant into multi bit FF as 2-bit FF, 4-bit FF and 8-bit FF are produced as a different assignment. At the point when will the obliged bit of capacity FF is required the specific errand is, no doubt brought in active region and others will be in-active (sleep mode) region.

In the proposed work it takes after that it is utilized to store the quantity of bits that are empowering specifically flip-flop utilizing single check and others are in sleep mode. It doesn't devour power for other flip-flop which is not empowered during the storage stage.

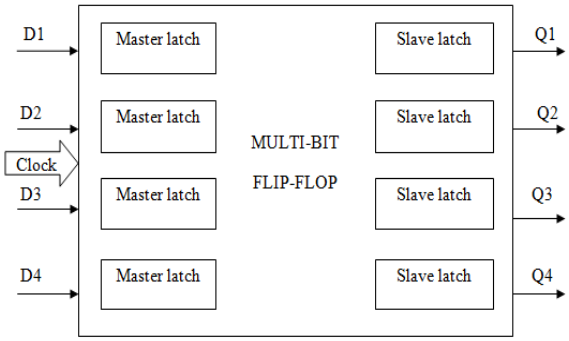

Fig. 2 Block diagram of MBFF

The multi smaller FF is supplanted by larger MBFF utilizing the less clock source; all the more over gadget varieties in the relating circuit can be successfully reduced. The FF can be fused with the assistance of combinational table which will be powerfully empowered built in light of the number of bit capacity necessity with force thought. The FF going to be united can be utilized for memory shows. By decreasing the quantity of Ffs, the clock sinks area and clock dynamic power have been viably diminished.

II.EXISTING METHOD

Ya-Ting Shyu et al [1] had utilized the numerous single bit flip- flop are supplanted by multi bit flip-flop. Because of this force is expanded and intricacy in configuration. The procedure [4] used to diminish control in the post-arrangement stage. In this work a chart based method is utilized within request to decrease the clock power. The flip-lemon is spoken to for every hub in the chart. The flip-failure relating to the hubs in an m-inner circle can be supplanted by an m-bit flip lemon. The calculation is utilized to discover m-coteries in a chart are extension and-bound and backtracking calculation. An alternate calculation is additionally used to discover the most extreme autonomous gathering of factions is ravenous heuristic calculation. In this work there is a probability of discovering outlandish mix of flip tumble in a library. Because of this it may prompt the wastage of time and more number of Ffs is utilized within every hub.

III.PROPOSED METHOD

In the past technique [1] the measure of time is wasted by discovering the impossible combination of FF furthermore numerous single bit FF is utilized. This may expand the complicated nature. So as to decrease the power MBFF idea is utilized. it portrays that need to recognize a legal placement region for every FF. In first stage, the reasonable

placement regions of a FF connected with diverse pins are discovered focused around the timing stipulations characterized on the pins. At that point, the legal placement region of the FF can be obtained by overlapped area of these regions.

Nonetheless, these regions are fit as a diamond shape; it is not simple to recognize the overlapped region. Accordingly, the overlapped zone can be recognized all the more effectively in the event that it can change the coordinate arrangement of cells to get rectangular regions. In the second stage, it might want to manufacture a combination table, which characterizes all combinations of FF keeping in mind the end goal to get another multi-bit Ffs given by the library.

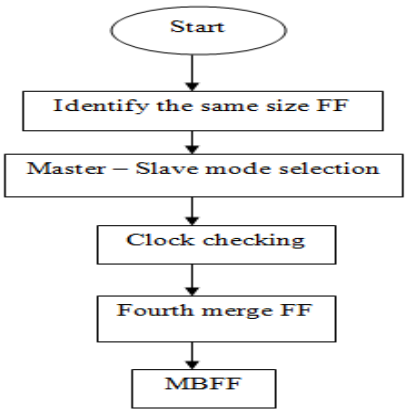

Fig.3 Flow-chart of merging flip-flop

The flip-flops can be united with the assistance of the table. After the legal placement regions of flip-flops are discovered and the combination table is fabricated, we can utilize them to merge flip-flops. To accelerate our project, we will isolate a chip into a few canisters and consolidation flip-flops in a neighborhood bin.

However, the flip-flops in diverse bins might be mergeable. In this way, we need to consolidate a few bins into a bigger bin and repeat this venture until no flip-flop can be fused any longer. In this area, we would detail each one phase of our technique. In the first subsection, we demonstrate a basic equation to change the original coordination framework into another one so that a legal placement region for each one flip-flop can be distinguished all the more effectively. The second subsection shows the flow of building the combination table. At long last, the substitutions of flip-flops will be depicted in the last subsection.

A.TRANSFORMATION OF PLACEMENT SPACE

The equations used to transform coordinate system are shown in (1) and (2). Suppose the location of a point in the original coordinate system is denoted by (*x, y).* After coordinate transformation, the new coordinate is denoted by (*x*", y"*).* In the original transformed equations, each value needs to be divided by the square root of 2, which would induce a longer computation time. Since we only need to know the relative locations of flip-flops, such computation are ignored in our method. Thus, we use *x*" and *y*", to denote the coordinates of transformed locations.

$$x' = \frac{x+y}{\sqrt{2}} \Rightarrow x'' = \sqrt{2}\,x' = x+y \longrightarrow (1)$$

$$y' = \frac{-x+y}{\sqrt{2}} \Rightarrow y'' = \sqrt{2}\,y' = -x+y \longrightarrow (2)$$

B.COMBINATION TABLE

A few flip-flops can be replaced by multi-bit flip-flop. In this proposed methodology, the combination table is assemble, which is utilized to get achievable flip-flops before substitution. This makes to use for recognizing the specific flip-flop which will be empowered in active region and cannot be covered. Utilizing this combination table, the flip-flop can be bit by bit replaced and this makes lessens the multifaceted nature of the configuration. Since one and only combination of flip-flop need to be considered in each one time, the clock signal can be successfully decreased.

IV APPLICATION DEVELOPED

The 1-bit, 2-bit, 4-bit and 8-bit Ffs are created as partitioned assignment as demonstrated in Fig. 3. The two inputs zone and b, is spoken to as input1 and b is spoken to as input2. These two inputs are included and put away in the FF updating. After that it checks the bits that are accessible in the area. The chosen Ffs are used when it is empowered and yield is shown. This makes decreases the power and delay in the design. The low power affects in the expense, size, weight, execution and unwavering quality.

The multiplier application can likewise be carried out in this proposed work. As opposed to including the bits, reproducing is possible and it is put away in the specific enabled flip-flop. For case, accept that a library just helps two sorts of flip-flops whose bit widths are 1 and 4 methods the specific flip-flop will be chosen and it will be empowered in the area and will be in sleep mode (in-active region).

The D-FF is utilized as a part of this proposed work. It gives synchronous information exchange and utilized for capacity reason. In any case, a dissimilar latch element, a FF just duplicates the information from the data pin to the yield once for every clock period and does not permit various multiple logic values to be passed in a clock cycle. Information is exchanged at either the rising or the falling clock edge, contingent upon the flip-flop

setup. Unlike latch, a FF is not level-sensitive, yet rather edge-activated. As it were, information gets put away into a FF just at the dynamic edge of the clock. The 16 bit FF can likewise be produced as indicated in Fig. 4; it diminishes the power and memory gadgets contrasted with single bit flip lemon. By and large, the snake libraries comprises AND, XOR as well as dominant part doors. The register banks are utilized to store the bit when it is enabled.

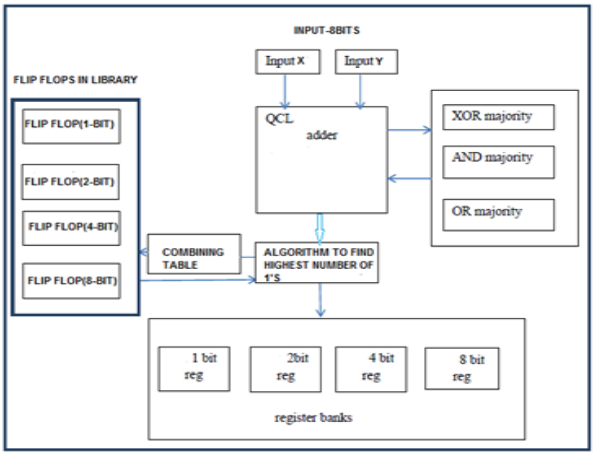

Fig. 4 Block diagram for MBFF used for application module

The D Flip-flop is the edge-triggered variation of the transparent latch. On the rising (typically, albeit negative edge triggering is possible) edge of the clock, this defer is given the estimation of the D data at that minute. This defer can be just change at the clock edge, and if the data changes at different times, the yield will be unaffected.

D flip-failures are by a wide margin the most well-known sort of flip-flops and a few gadgets are made altogether from D flip-flops. They are regularly utilized for shift- registers and input synchronization.

Objectives

1. Reduce the power consumption.
2. To reduce to the area.

3. To reduce the delay and power of a clock network.

4. To control clock skew because of common clock signal.

The above objectives can be achieved by merging several flip-flops and synchronizing with clock signals.

Quandary Statement

The following quandary statement has been identified:

1) Several Flip-flops needs a separate clock signal, hence Power consumption, is high.

2) Since several flip-flops needs a separate clock signal area consumed is also high.

V. BLOCK DIAGRAM AND ITS MODULES

This deals with the block diagram of the proposed method and its modules.

Block Diagram

The block diagram of the Application of Multi-bit flip-flop using QCL Adder as shown in figure 4.Two inputs are given to QCL adder. QCL adder are developed by Majority Logic XOR, AND, OR gate. The output of QCL adder is fed to highest bit "1" finding Algorithm. This Algorithm finds the number of bits and the combination table is built in order to merge the Flip-flops and it is stored in the Variable register banks.

Modules

This focuses on three different types of modules which are explained below.

1) Devise And Analysis Of Multi-Bit Flip-Flops

2) Devise Of Memory Device Using Multi-Bit Flip Flop

3) Devise and analysis of the application module

Devise and Analysis of Multi-Bit Flip-Flops

This module is utilized to decrease the power utilization by substituting some flip flop with less Multi-Bit flip flops. We are utilizing the Multi-Bit flip flop rather than more single bit flip flop to expand the clock synchronization. This will diminish the unnecessary force wastage through the utilization of numerous clock sinks.

Devise of Memory Device Using Multi-Bit Flip Flop

This is the application module to be developed. The memory designed by mainly using the multi-bit flip flops. In this, power consumption of memory devices is reduced compare to the single bit memory.

Analysis and Devise of the application Module

We are integrating all the sub modules and output signals are simulated.

VI. RESULTS

For the application module given above section was simulated. For adder, when clock leading edge input is 0 and the trailing edge input is 1, reset input is 1, input for a is 0000000 and the input for b is 01111111.The output is 01111111 as shown in the Fig below.

For example if the a input is 0000011 and if the b input is 0000011 the output will be 00000110 and the clock signal is given to the flip-flop that is required to show the output. The number of one's is two, so the two bit register was enabled the remaining flip-flops are in deactivation mode. By this we can reduce the power that is required for the operation in the system on chip.

COMPARISION TABLE

This table shows the delay and the power consumption by the clock utilization. The delay and clock power was almost same for all the designed flip-flops.

FF size	Delay(ps)	Clock Power(w)
1 bit	**0.487**	**0.017**
4 bit	**0.487**	**0.018**
8 bit	**0.487**	**0.018**

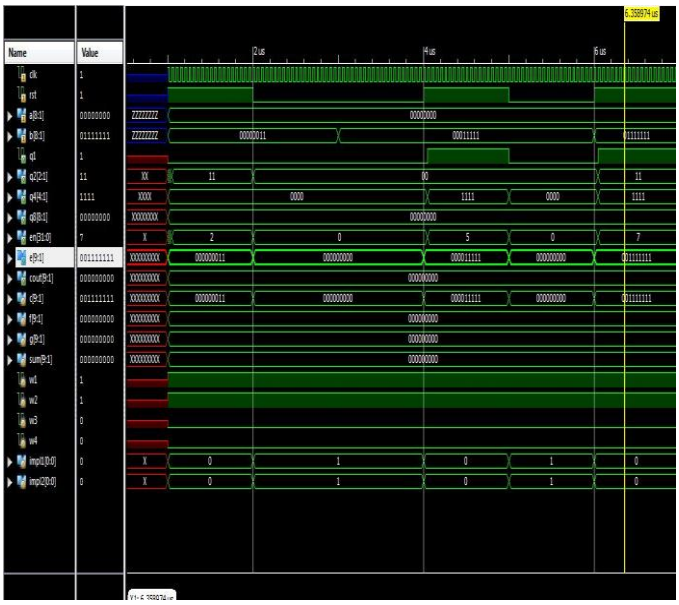

Fig. 5: shows simulation output of adder

VII. CONCLUSION

This project has proposed a methodology for flip-flop substitution for power reduction in digital integrated circuit design. The system of flip-flop substitutions is relying upon the combination table, which records the connections among the flip-flop types. By the rules of substitutions from the combination table, the incomprehensible combinations of flip-failures won't be viewed as that reductions execution time. Other than power reduction, the destination of minimizing the aggregate wire length likewise considered to the expense capacity. The verilog source code had produced for the application module as indicated in above areas and simulated utilizing the Isim test system. The single bit and multibit flip-flops source code additionally planned and reproduced and combined utilizing Xilinx ISE Design suite. This methodology can be appropriate for any circuit comprising of various flip-flops like counters registers.

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